DOCKET NO. 00-C-050 (STMI01-00050) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	William E. Ballachino
Application No.	:	09/667,164
Filed	:	September 21, 2000
For	:	M-BIT RACE DELAY ADDER AND METHOD OF OPERATION
Group No.	:	2193
Examiner	:	Chat C. Do
Confirmation No.	:	8138

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBSTITUTE APPEAL BRIEF

This is in response to the Notification of Non-Compliant Appeal Brief dated November 26, 2008.

The Appellant has appealed to the Board of Patent Appeals and Interferences from the final rejection of the Examiner dated February 20, 2008, finally rejecting claims 1-5, 8-16 and 19-31. The Appellant filed a Notice of Appeal on July 21, 2008, which was received by the Office on July 24, 2008. The Appellant respectfully submits this brief on appeal.

REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, STMICROELECTRONICS, INC.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1-5, 8-16 and 19-31 are pending and have been rejected by the final Office Action dated February 20, 2008. Claims 6-7 and 17-18 were canceled. Claims 1-5, 8-16 and 19-31 are presented for appeal.

STATUS OF AMENDMENTS

An Advisory Action mailed July 31, 2008 refused entry of amendments submitted following the final Office Action.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The following summary refers to disclosed embodiments and their advantages but does not delimit any of the claimed inventions.

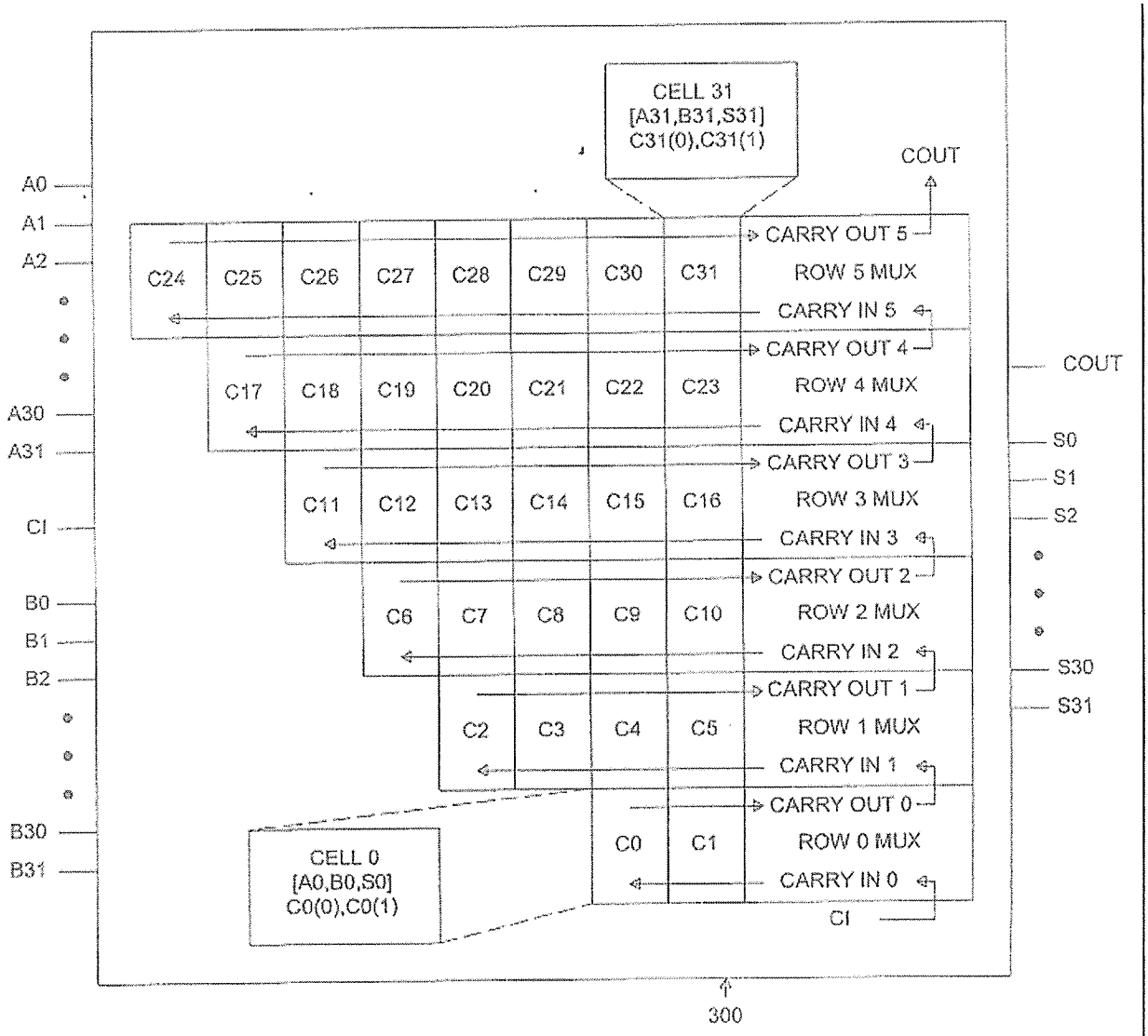
In General

The claimed subject matter relates generally to adder circuits.

Support for Independent Claims

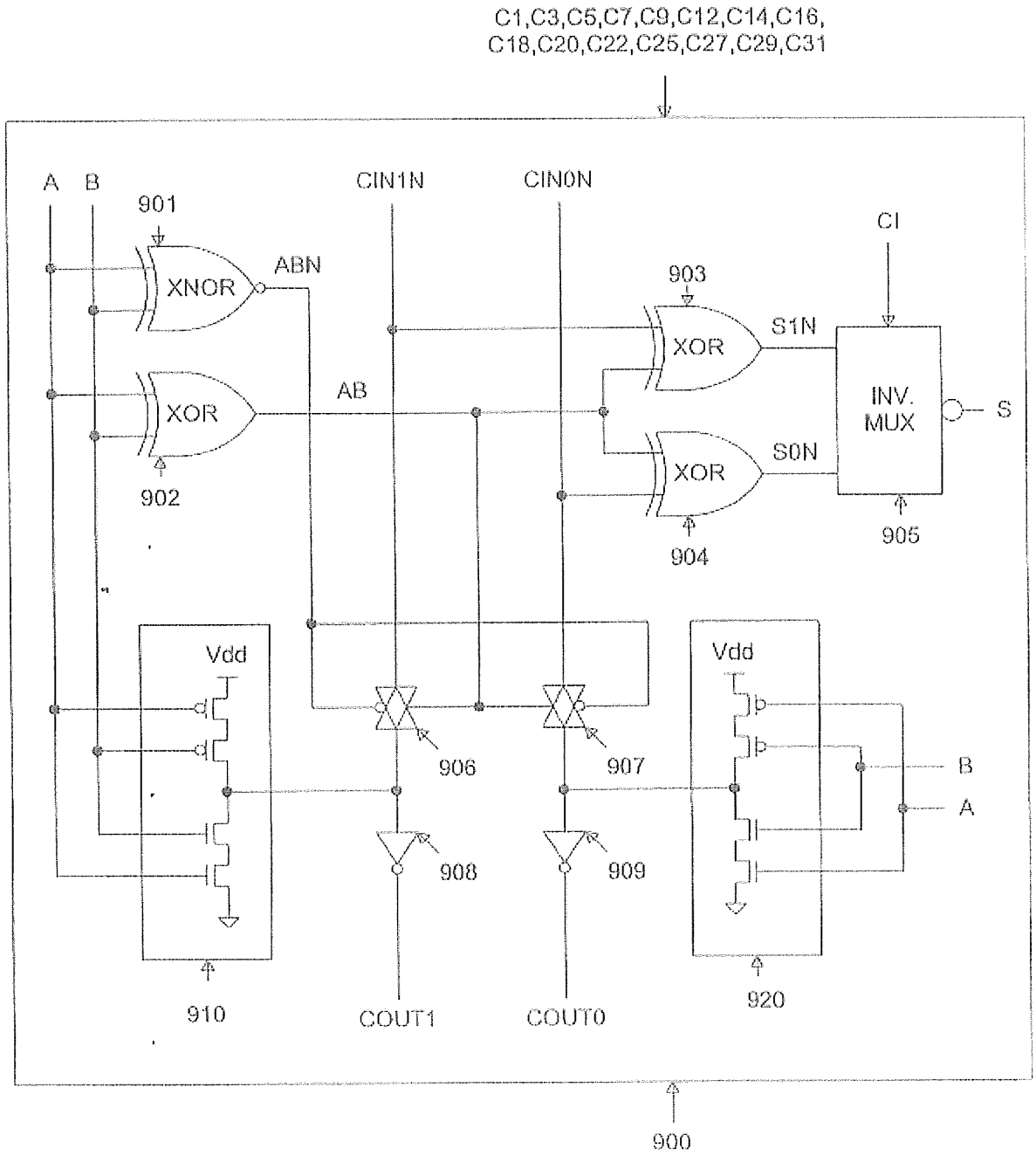
Note that, per 37 C.F.R. § 41.37, only the independent claims are discussed in this section. The discussion of the claims in this section is for illustrative purposes and is not intended to affect the scope of the claims.

In one embodiment, corresponding to independent claim 1, the claimed subject matter includes an M-bit adder 300 receiving a first M-bit argument A31-A0, a second M-bit argument B31-B0, and a carry-in bit CI:



Specification, Figure 3, page 16, lines 15-21. The M adder cells C0-C31 are arranged in R rows, wherein a least significant adder cell C2 in a first one of the rows receives a first data bit A_2 from the first M-bit argument and a first data bit B_2 from the second M-bit argument, generates both a first conditional carry-out bit $C_2(1)$ and a second conditional carry-out bit $C_2(0)$, and provides the

first and second conditional carry-out bits $C_2(1)$ and $C_2(0)$ to a second one C3 of the adder cells. Specification, page 17, line 5 to page 18, line 13. The $C_2(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells C0-C1 preceding the first row is a 1 and the $C_2(0)$ bit is calculated assuming the row carry-out bit from the second row is a 0. Specification, page 20, lines 12-21. The second one of the adder cells C3 within the first one of the rows receives a first data bit A_3 from the first M-bit argument and a first data bit B_3 from the second M-bit argument, receives both the first conditional carry-out bit $C_2(1)$ and the second conditional carry-out bit $C_2(0)$, and generates both a first conditional carry-out bit $C_3(1)$ and a second conditional carry-out bit $C_3(0)$ by propagating the first conditional carry-out bit $C_2(1)$ and the second conditional carry-out bit $C_2(0)$ through a first pass gate 906 and a second pass gate 907, respectively, when the first data bit A_3 and the second data bit B_3 are not equal, and outputs the first and second conditional carry-out bits $C_3(1)$ and $C_3(0)$ to other circuitry:



Specification, Figure 9, page 21, lines 4-14, page 36, line 22 to page 40, line 1.

In a second embodiment of the claimed subject matter, corresponding to independent claim 12, a data processor 106 includes an instruction execution pipeline with N processing stages each performing one of a plurality of execution steps associated with a pending instruction. At least one of the N processing stages comprises an M-bit adder 300 receiving a first M-bit argument A31-A0, a second M-bit argument B31-B0, and a carry-in bit CI. Specification, Figure 3, page 16, lines 15-21. The M adder cells C0-C31 are arranged in R rows, wherein a least significant adder cell C2 in a first one of the rows receives a first data bit A_2 from the first M-bit argument and a first data bit B_2 from the second M-bit argument, generates both a first conditional carry-out bit $C_2(1)$ and a second conditional carry-out bit $C_2(0)$, and provides the first and second conditional carry-out bits $C_2(1)$ and $C_2(0)$ to a second one C3 of the adder cells. Specification, page 17, line 5 to page 18, line 13. The $C_2(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells C0-C1 preceding the first row is a 1 and the $C_2(0)$ bit is calculated assuming the row carry-out bit from the second row is a 0. Specification, page 20, lines 12-21. The second one of the adder cells C3 within the first one of the rows receives a first data bit A_3 from the first M-bit argument and a first data bit B_3 from the second M-bit argument, receives both the first conditional carry-out bit $C_2(1)$ and the second conditional carry-out bit $C_2(0)$, and generates both a first conditional carry-out bit $C_3(1)$ and a second conditional carry-out bit $C_3(0)$ by propagating the first conditional carry-out bit $C_2(1)$ and the second conditional carry-out bit $C_2(0)$ through a first pass gate 906 and a second pass gate 907, respectively, when the first data bit A_3 and the second data bit B_3 are not equal, and outputs the

first and second conditional carry-out bits $C_3(1)$ and $C_3(0)$ to other circuitry. Specification, Figure 9, page 21, lines 4-14, page 36, line 22 to page 40, line 1.

In a third embodiment of the claimed subject matter, corresponding to independent claim 23, a method is disclosed of adding a first M-bit argument A31-A0, a second M-bit argument B31-B0 in an M-bit adder 300 comprising M adder cells C0-C31 arranged in R rows. Specification, Figure 3, page 16, lines 15-21. A first data bit A_2 from the first M-bit argument and a first data bit B_2 from the second M-bit argument are received in a least significant adder cell C2 in a first one of the rows of adder cells, which calculates a first conditional carry-out bit $C_2(1)$ and a first conditional sum bit $S_2(1)$ assuming a row carry-out bit from a second row of adder cells C0-C1 preceding the first row is a 1, and a second conditional carry-out bit $C_2(0)$ and a second conditional sum bit $S_2(0)$ assuming the row carry-out bit from the second row is a 0. Specification, page 17, line 5 to page 18, line 13. The $C_2(1)$ bit and the $C_2(0)$ bit are propagated to a second adder cell C3 in the first row of adder cells, and one of the $S_2(1)$ bit and the $S_2(0)$ bit are selected to be output from the least significant adder cell C2 according to a value of the row carry-out bit from the second row C0-C1. Specification, page 20, lines 12-21. A first data bit A_3 from the first M-bit argument and a first data bit B_3 from the second M-bit argument are received in the second adder cell C3 in the first one of adder cell rows, and the second adder cell C3 generates both a first conditional carry-out bit $C_3(1)$ and a second conditional carry-out bit $C_3(0)$ by propagating the first conditional carry-out bit $C_2(1)$ and the second conditional carry-out bit $C_2(0)$ through a first pass gate 906 and a second pass gate 907, respectively, when the first data

bit A_3 and the second data bit B_3 are not equal, and outputs the first and second conditional carry-out bits $C_3(1)$ and $C_3(0)$ to other circuitry. Specification, Figure 9, page 21, lines 4-14, page 36, line 22 to page 40, line 1.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Were claims 1-5, 8-16 and 19-31 properly rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter?

2. Were claims 1-5, 8-16 and 19-31 properly rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,682,303 to *Uya*?

ARGUMENT

1. GROUND OF REJECTION #1

Claims 1-5, 8-16 and 19-31 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

The final Office Action rejected claims 1-5, 8-16 and 19-31 as (a) merely disclosing a series of mental steps/components for adding two arguments without disclosing a practical/physical application, and (b) preempting every substantial practical application of the idea embodied by the claim. As best understood, the Advisory Action withdraws the portion of this rejection identified in (b) above, but maintains the portion identified in (a).

Claims 1-5, 8-16 and 19-31

Independent claims 1, 12 and 33 each recite (a) M adder cells, (b) the adder cells arranged in R rows, (c) the adder cells generating conditional carry-out bits and conditional sum bits, and (d) propagating the condition carry-out bits. These are hardware features recited within the claims, and preclude any determination that the claims are merely directed to "a series of mental steps/components."

The final Office Action offers no explicit interpretation of the term "adder cells," "rows" and/or "generating bits" that allows those limitations to be read on mental steps or components, nor any explanation of how those limitations may be satisfied by mental step or components. The rejection is therefore improper, since a proper rejection must be stated clearly and specifically. MPEP § 707.07(d), page 700-125 (8th ed. rev. 7, July 2008) ("Where a claim is

refused for any reason relating to the merits thereof it should be 'rejected' ***and the ground of rejection fully and clearly stated*** . . . ") (emphasis added).

Regardless, any such an interpretation is not supported by any evidence of record, and use of that interpretation is arbitrary and capricious. During prosecution, claims are given their broadest reasonable interpretation in light of the specification. MPEP § 2111, pages 2100-37 to 2100-38 (8th ed. rev. 7, July 2008). Under this mandate, claim terms are accorded their "plain meaning" – that is, the ordinary and customary meaning that the claim term would have to a person of ordinary skill in the art at the time of the invention – unless that plain meaning is inconsistent with the specification. MPEP § 2111.01(I) and (III), pages 2100-38 to 2100-40. However, the context in which the claim term is used in the specification should be considered in determining whether an interpretation accurately reflects the plain meaning of the claim term, together with evidence of customary usage by skilled artisans. MPEP § 2111.01(III), pages 2100-39 to 2100-40 ("It is the use of the words in the context of the written description and customarily by those skilled in the relevant art that accurately reflects both the 'ordinary' and the 'customary' meaning of the terms in the claims."). In particular, if more than one interpretation is possible based on "extrinsic" evidence (sources of support for an interpretation other than the specification), the specification must be consulted to determine which meaning is most consistent with applicant's use of the term(s). *Id.* at 2100-40. Only when more than one extrinsic definition is consistent with the use of the words in the specification can the claim terms be construed to encompass all such consistent meanings. *Id.*

Moreover, it is not sufficient to merely articulate a *conceivable* interpretation that might be accorded to claim terms, since the proper interpretation is limited to broadest *reasonable* interpretation. Accordingly, the interpretation adopted must find support in the evidence ("intrinsic" or "extrinsic") of record. *Dickinson v. Zurko*, 527 U.S. 150, 164 (1999) (review of Patent Office record-based factual findings governed by arbitrary and capricious, substantial evidence standards of Administrative Procedure Act, 5 U.S.C. § 706(2)(A), (E)); *In re Morris*, 127 F.3d 1048, 1055 (Fed. Cir. 1997). An agency decision that is not based on a consideration of relevant facts and which is a clear error of judgment (i.e., one that lacks rationality) is arbitrary and capricious. *In re Gartside*, 203 F.3d 1305, 1312 (Fed. Cir. 2005). An agency decision that is not supported by more than a mere scintilla of relevant evidence, sufficient for a reasonable mind to accept as adequate to support the conclusion and not consisting solely of mere uncorroborated hearsay or rumor, is not supported by substantial evidence. *Id.*

Claims 12-16 and 19-22

Independent claim 12 recites "an instruction execution pipeline" and "N processing stages, each . . . capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline." These additional hardware limitations preclude any determination that the claims are merely directed to "a series of mental steps/components." As with the limitations discussed above, no interpretation of these limitations allowing them to be read on mental steps/components is proffered in the Office Action, and any such interpretation is not supported by substantial evidence of record.

2. GROUND OF REJECTION #2

Claims 1-5, 8-16 and 19-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by *Uya.*

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-67 (8th ed. rev. 6 September 2007).

Claims 1-5, 8-16 and 19-31

As an initial matter, Applicants note that the interpretation of "pass gates" advanced in the Office Action is not supported by any evidence of record, such that use of that interpretation is arbitrary and capricious. The final Office Action states:

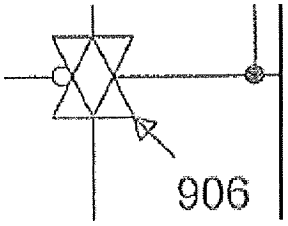
> [T]he claims do not define or address specifically what are the first and second pass gates respectively. Thus, as long as the cited reference discloses conditional carry-out bits are passing through logic gates, it would meet this claimed invention.

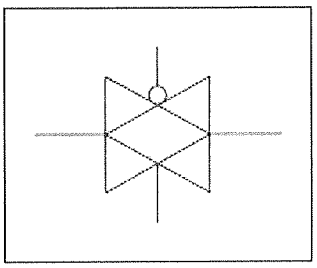
Paper No. 20080213, page 10. The Office Action thus interprets "pass gates" as encompassing any logic gate. This interpretation is not supported by any evidence of record and is inconsistent with usage of the term within the specification, and is therefore NOT "reasonable," such that reliance on the interpretation to reject the pending claims is arbitrary and capricious.

In the present matter, the Office Action identifies no basis for the interpretation proposed for "pass gates." The interpretation suggested is contrary to the specification, drawings and claims of the present application (the "intrinsic" evidence), which in every instance use the term

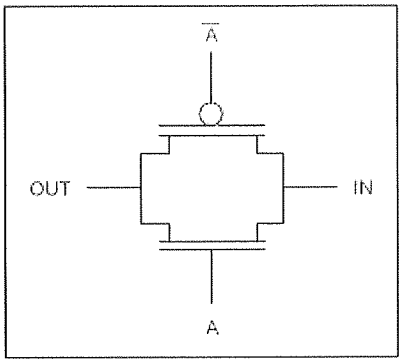
"pass gates" to refer to structures that are different from logic gates. For example, the specification and drawings use the term "pass gate" separately from "logic gate," and separately from specific logic gates such as inverters, NOT-AND (NAND) gates, NOT-OR (NOR) gates, exclusive-OR (XOR) gates and exclusive-NOR (XNOR) gates.

The Office Action neither asserts that the suggested interpretation of "pass gates" is based on any particular reference or other extrinsic evidence, nor identifies any evidence of record that "pass gates" is a particular term of art understood by those of ordinary skill to mean any logic gate. In fact, those skilled in the relevant art understand that pass gates are different from logic gates, ***since a different symbol is employed to represent pass gates than are used to represent the various logic gates***. Consistent with the circuit diagram conventions, the drawings depict the pass gates (also known as "transmission gates") with a known circuit symbol:





As known in the art, this symbol represents a pair of pMOS and nMOS transistors controlled by complimentary control signals applied to the transistor control gates so that both transistors are either on or off, that will selectively block (with high impedance) or pass a signal level from the input IN to the output OUT:



The above circuit symbol and the structure represented are well known in the art, and understood by those of ordinary skill. Only through deliberate ignorance can any other interpretation be ascribed to the term "pass gates" and the associated circuit symbol.

Because the suggested interpretation is not supported by any evidence of record (intrinsic or extrinsic) and is contrary to the meaning ascribed to the term "pass gates" in light of the specification and drawings, that interpretation is merely a conceivable interpretation, and not a reasonable interpretation supported by substantial evidence. In addition, to the extent that "pass gates" is actually used in the relevant art to refer to any and all logic gates, such a meaning is inconsistent with the usage of that term in the written description, where the term is employed solely to refer to controlled switches, structures that pass signal through substantially unchanged as described above. One skilled in the relevant art at the time the application was filed would therefore understand, in light of the specification and drawings, that the proper meaning of the term "pass gates" to most accurately read on switching structures that selectively pass signals through without inversion or other combination logic conditions, and NOT on any and all logic

gates. Accordingly the Office Action's reliance on that interpretation in rejecting the pending claims is arbitrary and capricious.

To the extent that the Office Action relies on the fact that logic gates may be implemented using pass gates therein as part of an unstated assertion of inherency, such reliance is improper. To establish inherency, the evidence must make clear that the feature is necessarily present in the process or structure described in the reference; the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency. MPEP § 2112(IV), page 2100-47. No evidence of record suggests that the logic gates 54 and 55 are implemented by pass gates.

Regardless, independent claims 1, 12 and 28 each recite that the recited pass gates propagate conditional carry-out bits $C_X(1)$ and $C_X(0)$ as conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$, respectively, when operand bits A_{X+1} and B_{X+1} are not equal. The NAND gate 54 and the inverter 55 of *Uya* do not propagate received conditional carry bits C^0_{25} and C^1_{25}, but instead compute a logical combination of C_{19}, C^0_{25} and C^1_{25}.

Moreover, independent claims 1, 12 and 28 each recite that the recited pass gates propagate conditional carry-out bits $C_X(1)$ and $C_X(0)$ as conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$, respectively, when operand bits A_{X+1} and B_{X+1} are not equal. The cited portion of *Uya* contains no logic conditioning the operation of NAND gate 54 and inverter 55 on a determination that bits A_{25} and B_{25} are not equal. To the extent that the Office Action relies on an unstated assertion that unconditionally compute a logical combination of C_{19}, C^0_{25} and C^1_{25}

(i.e., both when bits A_{25} and B_{25} are equal and when bits A_{25} and B_{25} are not equal), such an interpretation of the claims effectively reads the limitation "when operand bits A_{X+1} and B_{X+1} are not equal" completely out of the claims, giving that limitation no meaning whatsoever. Such an interpretation of the claims is arbitrary and capricious.

Finally, independent claims 1, 12 and 28 each recite that the second one of the adder cells within a particular row employ the recited pass gates to propagate conditional carry-out bits $C_X(1)$ and $C_X(0)$ as conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$, respectively, when operand bits A_{X+1} and B_{X+1} are not equal. NAND gate 54 and inverter 55 are not part of an adder cell within adders 50 and 51:

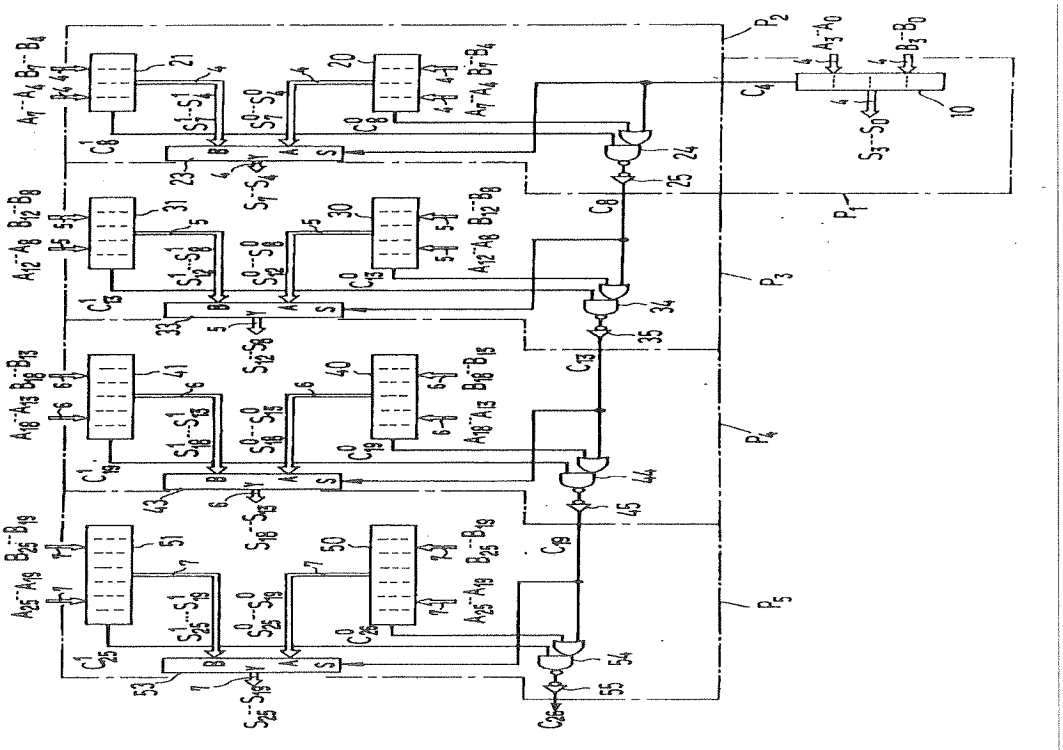


FIG. 2

As conceded in the Office Action in connection with claims 11 and 22, adders 50 and 51 are rows of adder cells within block adder P_5 (where block adder P_5 contains one more adder cell than block adder P_4, block adder P_4 contains one more adder cell than block adder P_3, etc.). NAND gate 54 and inverter 55 are not part of the adder cells within adders 50 and 51 that operate on bits A_{25} and B_{25}, and accordingly those adder cells within adders 50 and 51 that operate on bits A_{25} and B_{25} cannot be said to constitute a second adder cells within one of a plurality of rows of adder cells that is operable to generate both conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ by propagating conditional carry-out bits $C_X(1)$ and $C_X(0)$ through first and second pass gates, respectively, when data bits A_{X+1} and B_{X+1} are not equal.

CONCLUSION

All of the pending claims recite hardware features. Therefore, the rejection of the appealed claims under 35 U.S.C. § 101 is improper. The cited reference does not depict or describe all features of the claimed invention in the appealed claims. Therefore, the rejection under 35 U.S.C. § 102 is improper. Appellant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting the pending claims in the application.

Respectfully submitted,

MUNCK CARTER, P.C.

Date: 12-8-2008

Daniel E. Venglarik
Registration No. 39,409

Docket Clerk
P.O. Box 802432
Dallas, Texas 75380
Tel: (972) 628-3600
Fax: (972) 628-3616
Email : *dvenglarik@munckcarter.com*

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APPENDIX A

PENDING CLAIMS APPENDIX

1. An M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive a first data bit, A_X, from said first M-bit argument and a first data bit, B_X, from said second M-bit argument,

generate both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$,

provide the first and second conditional carry-out bits $C_X(1)$ and $C_X(0)$ to a second one of said adder cells, and

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0; and

wherein said second one of said adder cells in said first one of said rows is operable to:

receive a first data bit, A_{X+1}, from said first M-bit argument and a first data bit, B_{X+1}, from said second M-bit argument,

receive both said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$;

generate both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$, by propagating said first conditional carry-out bit, $C_X(1)$ and said

second conditional carry-out bit, $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal, and

output said first and second conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ to other circuitry.

2. The M-bit adder as set forth in Claim 1 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

3. The M-bit adder as set forth in Claim 2 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

4. The M-bit adder as set forth in Claim 3 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

5. The M-bit adder as set forth in Claim 4 wherein said other circuitry comprises:

a third adder cell in said first one of said rows of adder cells, and wherein said third adder cell receives a third data bit, A_{X+2}, from said first M-bit argument and a third data bit, B_{X+2}, from said second M-bit argument, and receives from said second adder cell said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit.

8. The M-bit adder as set forth in Claim 4 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

9. The M-bit adder as set forth in Claim 8 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

10. The M-bit adder as set forth in Claim 9 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

11. The M-bit adder as set forth in Claim 1 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

12. A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline, wherein at least one of said N processing stages comprises an M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit, said M-bit adder comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive a first data bit, A_X, from said first M-bit argument and a first data bit, B_X, from said second M-bit argument,

generate both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$,

provide the first and second conditional carry-out bits $C_X(1)$ and $C_X(0)$ to a second one of said adder cells, and

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row

carry-out bit from said second row is a 0; and

wherein said second one of said adder cells in said first one of said rows is operable to:

receive a first data bit, A_{X+1}, from said first M-bit argument and a first data bit, B_{X+1}, from said second M-bit argument,

receive both said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$;

generate both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$, by propagating said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal, and

output said first and second conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$.

13. The data processor as set forth in Claim 12 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

14. The data processor as set forth in Claim 13 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

15. The data processor as set forth in Claim 14 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

16. The data processor as set forth in Claim 15 wherein said other circuitry comprises:

a third adder cell in said first one of said rows of adder cells, and wherein said third adder cell receives a third data bit, A_{X+2}, from said first M-bit argument and a third data bit, B_{X+2}, from said second M-bit argument, and receives from said second adder cell said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit.

19. The data processor as set forth in Claim 15 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

20. The data processor as set forth in Claim 19 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

21. The data processor as set forth in Claim 20 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

22. The data processor as set forth in Claim 12 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

23. A method of adding a first M-bit argument and a second M-bit argument in an M-bit adder, the M-bit adder comprising M adder cells arranged in R rows, the method comprising the steps of:

receiving a first data bit, A_X, from the first M-bit argument and a first data bit, B_X, from the second M-bit argument in a least significant adder cell in a first one of the rows of adder cells;

calculating in the least significant adder cell a first conditional carry-out bit, $C_X(1)$, assuming a row carry-out bit from a second row of adder cells preceding the first row is a 1;

calculating in the least significant adder cell a second conditional carry-out bit, $C_X(0)$, assuming the row carry-out bit from the second row is a 0;

calculating in the least significant adder cell a first conditional sum bit, $S_X(1)$, assuming the row carry-out bit from the second row is a 1;

calculating in the least significant adder cell a second conditional sum bit, $S_X(0)$, assuming the row carry-out bit from the second row is a 0;

propagating the $C_X(1)$ bit and the $C_X(0)$ bit to a second adder cell in the first row of adder cells;

selecting one of the $S_X(1)$ bit and the $S_X(0)$ bit to be output from the least significant adder cell according to a value of the row carry-out bit from the second row; and

receiving a first data bit, A_{X+1}, from the first M-bit argument and a first data bit, B_{X+1}, from the second M-bit argument in the second adder cell in said first one of said rows of adder cells;

generating in said second adder cell both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$, by propagating said first conditional carry-out bit $C_X(1)$ and said second conditional carry-out bit $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal, and

outputting said first and second conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ to other circuitry.

24. The M-bit adder as set forth in Claim 1, wherein said second adder cell further comprises:

a first inverter operable for inverting said first conditional carry-out bit $C_X(1)$ transmitted through said first pass gate prior to outputting said first conditional carry-out bit $C_X(1)$; and

a second inverter operable for inverting said second conditional carry-out bit $C_X(0)$ transmitted through said second pass gate prior to outputting said second conditional carry-out bit $C_X(0)$.

25. The M-bit adder as set forth in Claim 1 wherein said second adder cell further comprises:

a first inverter operable for inverting said received conditional carry-out bit $C_X(1)$ prior to transmission through said first pass gate; and

a second inverter operable for inverting said received second conditional carry-out bit $C_X(0)$ prior to transmission through said second pass gate.

26. The M-bit adder as set forth in Claim 1 wherein said other circuitry comprises:

a row multiplexer, wherein said row carry-out bit from said second row of adder cells preceding said first row selects one of said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit to be output by said row multiplexer.

27. The M-bit adder as set forth in Claim 9 wherein said first adder cell comprises:

a first multiplexer operable for receiving said first conditional sum bit, $S_X(1)$ and said second conditional sum bit $S_X(0)$, wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said first adder cell; and

said second adder cell comprises:

a second multiplexer operable for receiving said second conditional sum bit $S_{X+1}(1)$ and said second conditional sum bit $S_{X+1}(0)$, wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

28. The data processor as set forth in Claim 12 wherein said second adder cell further comprises:

a first inverter operable for inverting said first conditional carry-out bit $C_X(1)$ transmitted through said first pass gate prior to outputting said first conditional carry-out bit $C_X(1)$; and

a second inverter operable for inverting said second conditional carry-out bit $C_X(0)$ transmitted through said second pass gate prior to outputting said second conditional carry-out bit $C_X(0)$.

29. The data processor as set forth in Claim 12 wherein said second adder cell further comprises:

a first inverter operable for inverting said received conditional carry-out bit $C_X(1)$ prior to transmission through said first pass gate; and

a second inverter operable for inverting said received second conditional carry-out bit $C_X(0)$ prior to transmission through said second pass gate.

30. The data processor as set forth in Claim 12 wherein said other circuitry comprises:

a row multiplexer, wherein said row carry-out bit from said second row of adder cells preceding said first row selects one of said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit to be output by said row multiplexer.

31. The data processor as set forth in Claim 20 wherein said first adder cell comprises:

a first multiplexer operable for receiving said first conditional sum bit, $S_X(1)$ and said second conditional sum bit $S_X(0)$, wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said first adder cell; and

said second adder cell comprises:

a second multiplexer operable for receiving said second conditional sum bit $S_{X+1}(1)$ and said second conditional sum bit $S_{X+1}(0)$, wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

DOCKET NO. 00-C-050 (STMI01-00050) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	William E. Ballachino
Application No.	:	09/667,164
Filed	:	September 21, 2000
For	:	M-BIT RACE DELAY ADDER AND METHOD OF OPERATION
Group No.	:	2193
Examiner	:	Chat C. Do
Confirmation No.	:	8138

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPENDIX B

EVIDENCE APPENDIX

None

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APPENDIX C

RELATED PROCEEDINGS APPENDIX

None